## REMARKS

In Item 3 of the Office Action mailed on December 14, 2004, Figure 1 was objected to. The Examiner asserted that Figure 1 should be labeled prior art. Figure 1 is so amended herewith in order to comply with this objection.

In Item 4 of the Office Action, the disclosure was objected to. The Examiner indicated that the serial number of the related application needs to be updated. Paragraph 2 of the specification is amended herewith to comply with this objection.

In Item 5 of the Office Action, claim 22 was objected to for an antecedent basis issue. Claim 22 is amended herewith to comply with this objection.

In Item 6 of the Office Action, claims 1-28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Nelson U.S. Patent 6,209,061. Claim 1 is directed to "a method for generating program overlays from a sequence of program code" and includes the following steps:

> (a) breaking the sequence of program code into a set of segments, wherein each segment contains a certain amount of related code for processing;
> (b) running a code segment in the set through a linker device;
> (c) extracting the code segment and related data segment produced by the linker device, with each associated pair of code and data segments representing an overlay;
> (d) checking if more segments exist in the set,
> if yes, then return to step (b), else proceed to step (e); and
> (e) concatenating the overlays into a file which can be referenced by the overlay manager.

Thus, steps (b) through (d) allow for the creation of multiple overlays, each comprising code and the data associated with that code, by utilizing multiple passes of the linker on multiple segments of code. The Examiner asserts that steps (b) through (d) are taught by the admitted prior art. In particular, the Examiner asserts that step (d) is taught by paragraph 16 in the "Background of the Invention" of the present application. Paragraph 16 states that "Prior implementations of overlays have used linker technology to create code and data segments that can be loaded into the processor memory area and executed." However, paragraph 16 goes on to say that "Such

prior implementations, however, have been configured to use only a single copy of a data segment in the main memory area. If multiple parts of the algorithm code need to use that particular data, these parts will be referred to the single copy in memory." Paragraph 16 nowhere refers to utilizing multiple passes of the linker on multiple segments of code. Using multiple passes of the linker in this way creates multiple overlays, each comprising a segment of code and the associated data. Therefore, a given segment of code does not have to "refer to the single copy (of a particular data segment) in memory," as is the case in the prior art described in paragraph 16, because the data associated with each block of code is included in that block of code's overlay.

The Examiner also asserts that step (e) of claim 1 is taught by Nelson. Specifically, the Examiner asserts that column 3, lines 10-19 teach "concatenating ... overlays into a file which can be referenced by the overlay manager," as called for in step (e) of claim 1. The cited portion of Nelson says that "overlay memory 23 can be segmented into a number of memory regions, with each region defined by a base pointer that evidences a base address of a region of addresses and a length value." This refers to the area of memory of the processor 21 that overlays can be loaded into when they are needed. This portion of Nelson says nothing about the process of generating overlays and, in particular, says nothing about forming an overlay file by concatenating multiple overlays (that have been generated in steps (a) through (d) of claim 1).

For at least the reasons outlined above, Applicant submits that claim 1, and claims 2-11 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.

Claim 12 was rejected for the same reasons used to reject claim 1. Therefore, Applicant submits that claim 12 is allowable for the reasons set out above with respect to claim 1. Applicant also submits that claim 12 further distinguishes from the admitted prior art and Nelson in that neither the admitted prior art nor Nelson teaches step (e): "importing symbols from the common code and linking the next individual code segment in the set of segments to produce an image." Thus, Applicant submits that claim 2, and claims 13-18 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.

Claim 19 was rejected for the same reasons used to reject claim 1. Therefore, Applicant submits that claim 19 is allowable for the reasons set out above with respect to claim 1. The Examiner further asserts that step (b) of claim 19, "creating an overlay control file for each overlay, whereby the overlay control file describes each pair of code and data associated with each overlay," is taught by Nelson at column 4, lines 5-10. Column 4, lines 5-10, of Nelson refer to an overlay memory controller 24, which holds the respective base pointers of the subregions of the overlay memory 23. Applicant submits that this overlay memory controller 24 does not does not constitute an overlay control file for each overlay, and in particular, an overlay control file that describes each pair of code and data associated with each overlay, as called for in claim 19. Applicant further points out that the overlays of Nelson consist of data only. See column 3, lines 6-9, which say, "Overlay memory 23 is a relatively small, high-speed memory which provides storage for data and parameters that are temporarily required for a program 26 that is currently running on CPU 12." In contrast, the overlays of the present invention comprise both code and data.

Applicant further points out that claim 19 contains numerous limitations that are not included in claim 1. Therefore, Applicant submits that it is not valid to reject claim 19 using a blanket statement that it is rejected for the same reasons as claim 1. In particular, Applicant submits that none of steps (a) through (j) are taught by either the admitted prior art or by Nelson. Applicant requests that the Examiner specifically point out the excerpts in the references that are deemed to teach these limitations. For at least the reasons laid out above, Applicant submits that claim 19, and claims 20-28 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.
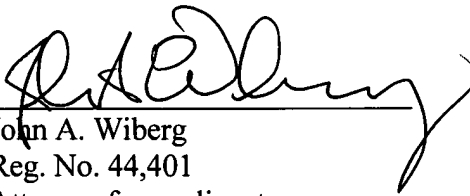
In view of the foregoing, Applicant respectfully requests reconsideration and allowance of claims 1-28.

Appl. No. 10/032,667
Amdt. dated Mar. 14, 2005
Reply to Office action of Dec. 14, 2004

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date:  <u>March 14, 2005</u>                          Respectfully submitted,


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**Amendments to the Drawings:**

The attached replacement drawing, FIG. 1, is amended to include the indication "(Prior Art)."